

What is claimed is:

1 1. A system for simulating a lithographic design comprised of a plurality of
2 polygons arranged in a predetermined configuration, the system comprising:

3 a microprocessor subsystem to convert the plurality of polygons to a pixel-
4 based bitmap representation thereof, wherein the pixel-based bitmap includes pixel
5 data, and wherein each pixel datum represents a pixel having a predetermined pixel
6 size; and

7 an accelerator subsystem, coupled to the microprocessor subsystem, to
8 calculate at least a portion of an aerial image of the lithographic design using the
9 pixel-based bitmap representation of the lithographic design, wherein the hardware
10 accelerator subsystem includes a plurality of programmable gate arrays configured
11 to process the pixel data in parallel.

1 2. The system of claim 1 wherein the pixel-based bitmap is a gray-level image
2 which is representative of the plurality of polygons.

1 3. The system of claim 1 wherein the predetermined pixel size is greater than
2 the Nyquist frequency in the aerial image of the lithographic design.

1 4. The system of claim 1 wherein the predetermined pixel size is determined
2 using the numerical aperture and wavelength of a projection optics of a lithographic tool.

1 5. The system of claim 1 wherein the lithographic design includes resolution
2 enhancement technology and wherein the microprocessor subsystem converts the plurality
3 of polygons, including resolution enhancement technology, to a pixel-based bitmap
4 representation thereof.

1 6. The system of claim 1 further including a plurality of accelerator subsystems,
2 each accelerator subsystem being coupled to the microprocessor subsystem and provided
3 a portion of the pixel-based bitmap to calculate an aerial image of the lithographic design
4 corresponding to the portion of the pixel-based bitmap using the pixel data associated
5 therewith.

1 7. The system of claim 6 wherein the microprocessor subsystem includes a
2 plurality of microprocessors and wherein each microprocessor is coupled to at least one
3 associated accelerator subsystem.

1 8. The system of claim 7 wherein the plurality of accelerator subsystems each
2 performs Fast Fourier Transforms, using pixel data, to generate the corresponding portion
3 of the aerial image.

1 9. The system of claim 1 wherein the accelerator subsystem calculates an aerial
2 image in resist formed on a wafer by the lithographic design wherein the accelerator
3 subsystem calculates the aerial image in resist using the pixel-based bitmap representation

4 of the lithographic design and a coefficient matrix representing projection and illumination
5 optics of a lithographic tool.

1 10. The system of claim 9 wherein the accelerator subsystem calculates a pattern
2 formed on the wafer by the lithographic design wherein the accelerator subsystem
3 calculates the pattern on the wafer using the pixel-based bitmap representation of the
4 lithographic design and the coefficient matrix representing projection and illumination optics
5 of a lithographic tool.

1 11. The system of claim 10 further including a processing system, coupled to the
2 microprocessor subsystem and the accelerator subsystem, to compare the calculated
3 pattern on the wafer to a desired, predetermined pattern.

1 12. The system of claim 10 further including a processing system, coupled to the
2 microprocessor subsystem and the accelerator subsystem, to determine a CD of the
3 lithographic design using the calculated pattern on the wafer.

1 13. The system of claim 10 further including a processing system, coupled to the
2 microprocessor subsystem and the accelerator subsystem, to determine an edge
3 placement of the lithographic design using the calculated pattern on the wafer.

1 14. The system of claim 10 further including a processing system, coupled to the
2 microprocessor subsystem and the accelerator subsystem, to determine a printing

3 sensitivity using patterns on the wafer calculated in response to varying the coefficients of
4 the matrix representing projection and illumination optics of a lithographic tool.

1 15. The system of claim 14 wherein the coefficients of the matrix representing
2 projection and illumination optics of a lithographic tool are representative of one or more of
3 a focus, dose, numerical aperture, illumination aperture, and aberration.

1 16. The system of claim 15 wherein the processing system determines a set of
2 parameters of the projection and illumination optics of the lithographic tool using the
3 printing sensitivity.

1 17. The system of claim 10 further including a processing system, coupled to the
2 microprocessor subsystem and the accelerator subsystem, to detect an error in the
3 lithographic design in response to a comparison between the calculated pattern on the
4 wafer and a desired, predetermined pattern.

1 18. The system of claim 17 wherein, in response to detecting the error, the
2 processing system determines a modification to the lithographic design to correct the error
3 in the lithographic design.

1 19. A system for simulating a lithographic design, the system comprising:
2 a microprocessor subsystem, including a plurality of microprocessors, to
3 convert the lithographic design to a pixel-based bitmap representation thereof,

4 wherein the pixel-based bitmap includes pixel data, and wherein each pixel datum
5 represents a pixel having a predetermined pixel size; and

6 a plurality of accelerator subsystems, each accelerator subsystem includes a
7 plurality of programmable integrated circuits configured to process the pixel data in
8 parallel and each accelerator subsystem is connected to an associated
9 microprocessor to calculate a portion of an aerial image of the lithographic design
10 using the corresponding portion of the pixel-based bitmap representation of the
11 lithographic design.

1 20. The system of claim 19 wherein the lithographic design is comprised of a
2 plurality of polygons arranged in a predetermined configuration.

1 21. The system of claim 20 wherein the pixel-based bitmap is a gray-level image
2 which is representative of the plurality of polygons.

1 22. The system of claim 19 wherein the predetermined pixel size is greater than
2 the Nyquist frequency in the aerial image of the lithographic design.

1 23. The system of claim 19 wherein the predetermined pixel size is determined
2 using the numerical aperture and wavelength of a projection optics of a lithographic tool.

1 24. The system of claim 19 wherein the lithographic design includes resolution
2 enhancement technology and wherein the microprocessor subsystem converts the plurality

3 of polygons, including resolution enhancement technology, to a pixel-based bitmap
4 representation thereof.

1 25. The system of claim 19 wherein the plurality of accelerator subsystems each
2 performs Fast Fourier Transforms, using pixel data, to generate the corresponding portion
3 of the aerial image.

1 26. The system of claim 19 wherein the plurality of accelerator subsystems
2 calculate an aerial image in resist formed on a wafer by the lithographic design, wherein the
3 accelerator subsystems calculate the aerial image in resist using the pixel-based bitmap
4 representation of the lithographic design and a coefficient matrix representing projection
5 and illumination optics of a lithographic tool.

1 27. The system of claim 26 wherein the accelerator subsystems calculate a
2 pattern formed on the wafer by the lithographic design wherein the accelerator subsystems
3 calculate the pattern on the wafer using the pixel-based bitmap representation of the
4 lithographic design and the coefficient matrix representing projection and illumination optics
5 of a lithographic tool.

1 28. The system of claim 27 further including a processing system, coupled to the
2 microprocessor subsystems and the accelerator subsystems, to compare the calculated
3 pattern on the wafer to a desired, predetermined pattern.

1 29. The system of claim 27 further including a processing system, coupled to the
2 microprocessor subsystems and the accelerator subsystems, to determine a CD of the
3 lithographic design using the calculated pattern on the wafer.

1 30. The system of claim 27 further including a processing system, coupled to the
2 microprocessor subsystems and the accelerator subsystems, to determine an edge
3 placement of the lithographic design using the calculated pattern on the wafer.

1 31. The system of claim 27 further including a processing system, coupled to the
2 microprocessor subsystems and the accelerator subsystems, to determine a printing
3 sensitivity using patterns on the wafer calculated in response to varying the coefficients of
4 the matrix representing projection and illumination optics of a lithographic tool.

1 32. The system of claim 31 wherein the coefficients of the matrix representing
2 projection and illumination optics of a lithographic tool are representative of one or more of
3 a focus, dose, numerical aperture, illumination aperture, and aberration.

1 33. The system of claim 32 wherein the processing system determines a set of
2 parameters of the projection and illumination optics of the lithographic tool using the
3 printing sensitivity.

1 34. The system of claim 27 further including a processing system, coupled to the
2 microprocessor subsystems and the accelerator subsystems, to detect an error in the

3 lithographic design in response to a comparison between the calculated pattern on the
4 wafer and a desired, predetermined pattern.

1 35. The system of claim 34 wherein, in response to detecting the error, the
2 processing system determines a modification to the lithographic design to correct the error
3 in the lithographic design.